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(71) Applicant: N.V. Philips' Gloeilampenfabrieken
Groenewoudseweg 1
NL-5621 BA Eindhoven(NL)

(72) Inventor: Veldhuis, Raymond Nicolaas Johan
c/o Int. Octrooibureau B.V., Prof. Holstlaan 6
NL-5656 AA Eindhoven(NL)
Inventor: Keesman, Gerrit Johan
c/o Int. Octrooibureau B.V., Prof. Holstlaan 6
NL-5656 AA Eindhoven(NL)

(74) Representative: Groenendaal, Antonius Wilhelmus Maria et al
Internationaal Octrooibureau B.V. Prof. Holstlaan 6
NL-5656 AA Eindhoven (NL)

(54) Device for transmitting data words representing a digitized analog signal.

(57) A transmission system is disclosed for transmitting digitized analog information. At the transmission side, for the purpose of transmitting an additional information signal, data words representing the digitized information are modified depending on the bits of an additional information signal. The modifying means (21,22) are constructed in such a way that the modification depends both on the additional information signal and on other bits (b7) which are not correlated with the bits (d) of the additional information signal. This results in the intercorrelation between the errors (Δ, e) in the data words introduced by the modification being reduced, so that a flatter power density error spectrum is obtained and the errors introduced in the data words by the modification are less conspicuous.

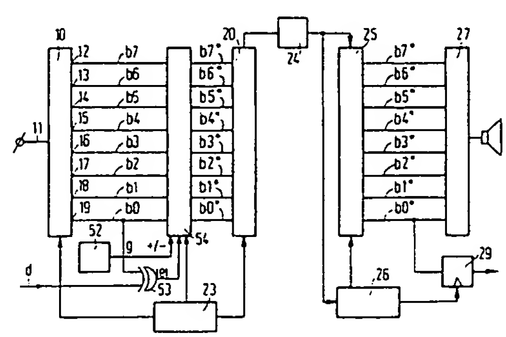

FIG.3

EP 0 545 915 A2

The invention relates to a device for transmitting a series of data words representing a digitized analog signal, which device comprises modifying means constructed to modify the series of data words, prior to transmission, in dependence upon an additional information signal in such a way that after modification the additional information signal is represented by less significant bits of selected data words, the values represented by the modified data words being slightly different from the values represented by the relevant data word prior to modification.

Such device is known from European Patent Application EP-A-0,205,200.

Said Application describes a transmission system in which for the transmission of the additional information signal one or more of the least significant bits of every n-th signal sample of a series of digitized audio samples is or are replaced by bits of the additional information signal. After the series of signal samples thus modified has been transmitted the additional information signal is recovered from the signal samples, the original audio signal being recovered from the signal samples by digital-to-analog conversion.

The substitution of the least significant bits in every n^{th} signal sample introduces a minor error in the signal values. If the logic value of the additional information signal remains constant for a longer time repetition patterns may arise in the errors, resulting in audible whistle tones in the recovered audio signal. This is caused by the fact that the errors are intercorrelated if the additional information signals do not vary significantly.

In the known method the occurrence of annoying whistle tones is precluded in that, after recovery of the additional information signal, the signal sample bits are used for the transmission of the additional information signal are replaced by a bit of an arbitrary logic value, which substantially reduces the correlation in the consecutive errors. However, this known method has the drawback that additional circuits are needed in the signal processing path where the received signal samples are converted into the original audio signal. This is undesirable, in particular if the number of receiving devices is substantially larger than the number of transmitting devices, as for example in the case that the information is transmitted via a record carrier, such as for example a magnetic tape or an optically readable disc.

Further GB-A-1203768 discloses a device for transmitting a digital representation of an analog signal (speech) and an additional information signal (telegraph) over a single telecommunications channel. The device comprises modifying means constructed to modify the series of bits representing the analog signal prior to the transmission depending on the additional information signal. Insertion of additional information bits is carried out by replacing bits representing the analog signal (bit-stealing) and is carried out intermittently so that the transmitted analog signal is not substantially affected. For the reduction of the perceptibility of the effects of additional information signal insertion the modifying means are adapted to modify the series of bits representing the analog signal depending both on the additional information signal and on the logic values of other bits than the replaced bits. The modification depends on the values of bits adjacent to the replaced bit which adjacent bits are not correlated with the additional information signal.

Furthermore, transmission of digitized analog signals arranged in a series of data words together with additional information signals by using "bit-stealing" is known from GB-A-2063018.

It is the object of the invention to provide means which enable information to be transmitted by means of a device as defined in the opening paragraph, in such a way that the correlation in the consecutive errors is reduced without additional circuits being needed in the signal processing path of the signal samples at the reception side, and in which the additional information signal can be directly recovered from the less significant bits.

This object is achieved by a device which is characterized in that the modifying means are adapted to modify the selected data words depending both on the additional information signal and on the logic values of other bits than said less significant bits, which other bits are non-correlated with the additional information and in that the modifying means comprise means for changing the values represented by the selected data words in such a way that after the change the n least significant bits of each of the relevant data words correspond to the logic value of n bits of the information signal, and means for determining the signs of the changes depending on the logic values of said other bits.

An embodiment of the transmitting device is characterized in that the device comprises a binary wide-noise generator for generating said other bits.

Further embodiments of the transmitting device and the receiving device and their advantages will now be described in more detail, by way of example, with reference to Figures 1 to 6, of which

Figures 1 and 2 serve to illustrate prior-art methods of transmitting an additional information signal,

Figures 3 and 6 show transmission systems utilizing different embodiments of the transmitting device and of the receiving device in accordance with the invention,

Figure 4 illustrates the data-words modification dependent upon the additional information signal

for different embodiments of the transmitting device in accordance with the invention, and

Figure 5 illustrates the relationship between the prevailing error and the logic values of bits of the data word and the additional information word for different embodiments of a transmitting device in accordance with the invention.

Figure 1 shows a series 1 of 8-bit data words, representing a series of digitized signal samples of an analog signal, for example an audio or a video signal. The reference numeral 2 indicates a series of data words derived from the series 1 by replacing the least significant bit b0 of every third data word (in Figure 1 these are the least significant bits of the 2nd, 5th, 8th, 11th, 14th and 17th data word) by a bit of an additional information signal comprising a series 3 of bits d5, ..., d0.

The series 2 of modified data words can subsequently be transmitted via a customary data transmission channel or a record carrier. After transmission the additional information signal can be recovered by detecting the least significant bits of every nth data word received. The analog signal represented by the data word can be recovered from the series of data words by customary digital-to-analog conversion techniques. This method of transmitting additional information along with the digitized analog information is frequently referred to as "bit-stealing".

Transmitting additional information by means of bit-stealing has the advantage that the data format used for the transmission need not be modified.

Since for the transmission only the least significant bits of the data words are used the error introduced in the recovered analog signal as a result of bit-stealing is minimal. Figure 2 by way of illustration gives the magnitude of the error Δ as a function of the logic value of the least significant bit b0 of the original data word and the logic value of the bit d of the additional information.

If the additional information varies only to a small extent repetition patterns may arise in the errors Δ, which in the case that the analog signal is an audio signal result in audible whistle tones and in the case that the analog signal is a video signal result in a visible interference pattern in the video picture. This is caused by the fact that the errors Δ are intercorrelated and the spectral power density distribution of the error signal consequently exhibits peaks.

In the embodiments to be described hereinafter steps have been taken to reduce the intercorrelation between the errors, which results in a flatter spectral power density distribution and hence in less conspicuous errors in the audio or the video signal.

Figure 3 shows an information transmission system employing a first embodiment of a transmitting device and a receiving device in accordance with the invention. The reference numeral 10 denotes an analog-to-digital converter by means of which an analog signal, for example and audio or a video signal, applied via an input 11 is converted into data words, for example 8-bit data words. The individual bits of the data words are referred to as b7, ..., b0, where b7 is the most significant bit and b0 is the least significant bit.

The bits b7, ..., b0 are fed out via the respective outputs 12, ..., 19. The output signals on the outputs 12, ..., 19 to an arithmetic circuit 54. The outputs of circuit 54 are applied to the parallel inputs of a signal processing circuit 20.

The processing circuit 20 in a customary manner converts the data words which are applied in parallel form into a serial bit stream, synchronization signals being inserted into the bit stream for the purpose of synchronizing the information transmission.

The processing circuit 20 may comprise for example known circuits as used for recording standard CD signals or standard DAT signals. By means of a clock signal generator 23 the signal processing circuit 20 and the analog-to-digital converter 1-and the circuit 54 are controlled in such a way that the least significant bit of every nth data word is replaced by a bit having a logic value equal to a bit d of the additional data word.

Figure 3 also shows the circuit for recovering the additional information signal. In the circuit the bit series transmitted via a transmission channel or transmission medium 24, for example a DAT cassette tape or an optical storage medium, is applied to a second processing circuit 25 and a synchronizing circuit 26. The synchronizing circuit, in a manner known per se, detects the synchronizing signals in the received bit stream to derive clock signals for controlling the processing circuit 25, which recovers the data words from the serial bit stream. The bits b7, ..., b1 and b0* are applied to a digital-to-analog converter 27, which reconverts the data words into an analog signal. The bit b0* is also applied to the input of a flip-flop 29, which is controlled by the synchronizing circuit 26 in such a way that upon reception of every nth data word the flip-flop 29 is loaded with the bit b0* so that the additional information signal becomes available on the output of the flip-flop 29.

In the circuit shown in Figure 3 the data words are converted into a series of serial bits. However, it will be evident that, although this is common practice in information transmission, it is not necessary to convert the data words into serial form but that the information may also be transmitted in parallel form.

In the circuit shown in Figure 3 only one bit of every nth data word is replaced. However, it is

equally possible to replace more than one bit in every n^{th} data word.

In the present embodiment every n^{th} data word of the series 1 of data words is incremented or decremented by such a modification value that the least significant bit of the modified data word corresponds to the logic value of one bit of the additional information signal to be transmitted.

Before the circuit shown in Figure 3 is described further in detail the underlying bit-stealing method will be described with reference to Figure 4.

In Figure 4 the series of data words generated by the analog-to-digital converter 10 again bears the reference numeral 1 and the series of bits d of the additional information signal again bears the reference numeral 3. The reference numeral 50 denotes the series of data words in which every third data word is changed by a modification value e. The modification value e is derived from the least significant bit b0 in data words to be modified and the bit d of the additional information word to be transmitted, in such a way that after modification the logic value of the least significant bit corresponds to the logic value of the bit d to be transmitted. If, as is the case for the second, the eight and the seventeenth data word of the series 30, the logic value of the least significant bit 60 and the logic value of the bit d to be transmitted are equal to data word need not be modified, i.e. the modification value e is zero. If, as is the case for the fifth, the eleventh and the fourteenth data word of the series 1, the logic value of the least significant bits b0* and the bits d do not correspond, a modified data word whose least significant bit b0 corresponds to the bit d can be obtained by incrementing or decrementing the data word by the value one. In order to minimize the intercorrelation between the consecutive values e, i.e. the errors introduced by bit-stealing, an arbitrary sign is selected for the modification.

In Figure 4 this sign is determined by a series 51 of bits g of arbitrary logic value.

In the transmission system shown in Figure 3 the series 51 is generated by means of a binary random-noise generator 52 of a customary type, the absolute value of e being derived from the bits d of the additional information signal and the least significant bits b0 of the data words by means of an Exclusive-OR gate 52. For modifying the data words the arithmetic circuit 54 of a customary type is arranged between the analog-to-digital converter 10 and the processing circuit 20, which arithmetic circuit is controlled in dependence on the output signal of binary noise generator the output signal of the Exclusive-OR gate 53 and the clock signal on the output of generator 23, in such a way that every n^{th} data word is incremented or decremented by the value indicated by the output signal |e| of the Exclusive-OR gate 53, depending on the output signal of the binary noise generator 52.

This yields a series of data words in which the least significant bits of every n^{th} data word corresponds to a bit of the additional information signal.

At the receiving side the bits d of the additional information signal can be detected simply by means of the flip-flop 29 which is controlled by the synchronizing circuit 26, the least significant bit b0* being applied directly to the data input of the flip-flop.

In the embodiment shown in Figure 3 the sign of the modification is determined by means of the binary noise generator 52. Since the data word bits b0, ..., b7 are non-correlated with the bits d of the additional information signal these bits can also be used for determining the sign of the modification, which yields a very simple embodiment of the receiver.

Further, the embodiment shown in Figure 3 only employs the least significant bit of every n^{th} data word for the transmission of the additional information signal. However, it is alternatively possible to use two or more bits of the data word for this purpose. Figure 5 by way of example illustrates the relationship between the modification value e, the arbitrary bit g, the two least significant bits 61, 60 and two bits d, d* of the additional information signal.

Figure 5 shows that for specific combinations of b1, b0 and d, d*, for example b1, b0, d, d* = (0,0,0,1), the sign of the modification is independent of g. For said combination b1, b0, d, d* = (0,0,0,1) the modification values always +1. However, for a number of other combinations, namely b1, b0, d, d* = (0010), (0111), (1000), and (1101) the sign may be selected freely. For these combinations the data words with the bits b1* and b0*, whose logic values correspond to those of the data bits d, d* can be obtained by a modification by +2 or by -2. If the sign of the modification is now made dependent on the bits g of arbitrary logic values the intercorrelation between the successive errors, i.e. the value of e, can be reduced.

Figure 6 shows a variant of the circuit shown in Figure 9 by means of which the data words are incremented or decremented in accordance with the last-mentioned modification method. The Exclusive-OR gate 53 is replaced by a circuit 60, which derives the absolute magnitude of the modification value e and the sign of the modification from the bits g of the arbitrary series, the two least significant bits b1, b0 of the data word, and the bits d, d* of the additional information signal. The absolute magnitude of the modification value and the sign of the modification are transferred to the

arithmetic circuit 54 via a bus 61 and a signal line 62 respectively. The circuit 60 may comprise a read-only memory (ROM) or a gate circuit which defines the relationship illustrated in Figure 5.

In the last-mentioned method in the rare situation in which the original data words already have the maximum positive or maximum negative value a relative overflow situation may arise. If desired, this can be precluded by detecting data words of maximum positive or maximum negative value and subsequently, depending on the sign, decrementing instead of incrementing, or incrementing instead of decrementing.

Claims

1. A device for transmitting a series of data words representing a digitized analog signal, which device comprises modifying means constructed to modify the series of data words prior to the transmission depending on an additional information signal (d) in such a way that after modification the additional information signal is represented by less significant bits (bo') of the selected data words (2), the values represented by the modified data words being slightly different from the values represented by the relevant data words (1) prior to modification, characterized in that the modifying means are adapted to modify the selected data words depending both on the additional information signal and on the logic values of other bits than said less significant bits, which other bits are non-correlated with the additional information and in that the modifying means comprise means (54) for changing the values represented by the selected data words in such a way that after the change the n least significant bits of each of the relevant data words correspond to the logic value of n bits of the information signal, and means (53) for determining the signs of the changes depending on the logic values of said other bits.

2. A device as claimed in Claim 1, characterized in that the device comprises a binary-random-noise generator (52) for generating said other bits.

3. A transmitting device as claimed in Claim 1 or 2, characterized in that the modification value and n are both equal to one.

3

d5	d4	d3	d2	d1	d0
1	0	0	1	1	0

	b7	b6	b5	b4	b3	b2	b1	b0
1	1	0	0	0	0	0	1	1
2	0	0	0	1	1	0	0	1
3	0	0	1	0	0	0	1	0
4	0	0	1	1	1	0	0	1
5	0	1	0	0	1	1	1	1
6	0	1	1	0	0	1	0	1
7	0	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	0
9	1	1	0	0	1	0	0	1
10	0	1	1	1	1	1	0	1
11	0	1	0	1	1	0	1	0
12	0	1	0	0	0	1	0	0
13	0	0	0	1	1	1	1	0
14	0	0	0	0	1	1	1	0
15	0	0	0	1	0	0	0	0
16	0	0	0	1	1	1	0	1
17	1	0	0	0	0	0	0	0
18	1	0	0	0	1	1	0	1

1

b7	b6	b5	b4	b3	b2	b1	b0*
1	0	0	0	0	0	1	1
0	0	0	1	1	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	1	0	0	1
0	1	0	0	1	1	1	0
0	1	1	0	0	1	0	1
0	1	1	1	0	0	0	0
1	0	0	0	1	1	1	0
1	1	0	0	1	0	0	1
0	1	1	1	1	1	0	1
0	1	0	1	1	0	1	1
0	1	0	0	0	1	0	0
0	0	0	1	1	1	1	0
0	0	0	0	1	1	1	1
0	0	0	1	0	0	0	0
0	0	0	1	1	1	0	1
1	0	0	0	0	0	0	0
1	0	0	0	1	1	0	1

2

FIG.1

b0	d	b0*	△
0	0	0	0
1	0	0	-1
0	1	1	1
1	1	1	0

b0* = d

FIG.2

b1, b0 \ b1*, b0* = d,d*	00	01	10	11
00	0	+1	+2	−1
01	−1	0	+1	+2
10	+2	−1	0	+1
11	+1	+2	−1	0

g = 1

b1, b0 \ b1*, b0* = d,d*	00	01	10	11
00	0	+1	−2	−1
01	−1	0	+1	−2
10	−2	−1	0	+1
11	+1	−2	−1	0

g=−1

FIG.5

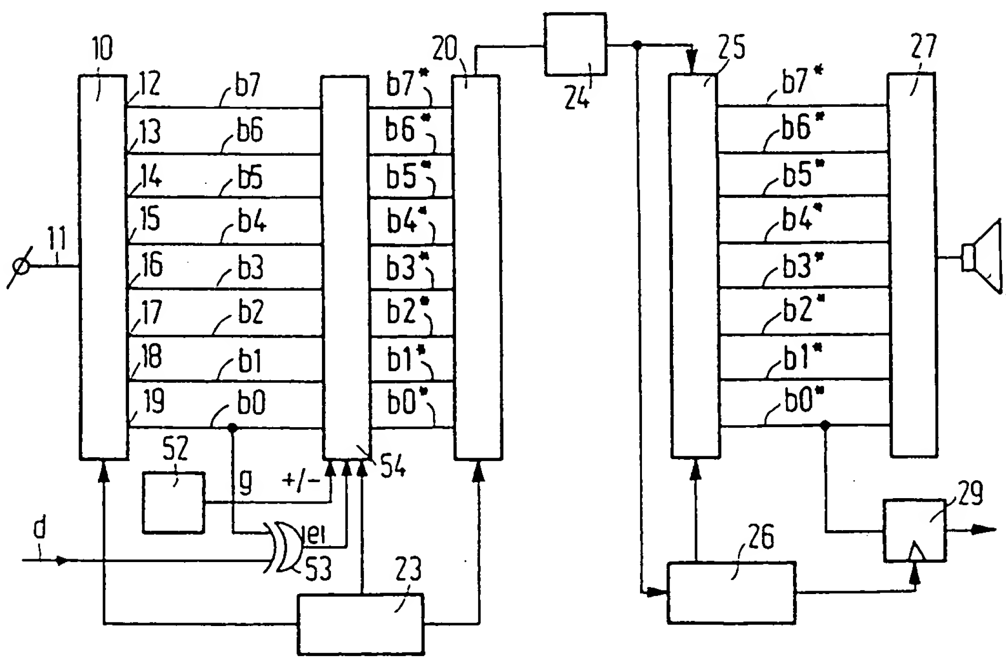

FIG.3

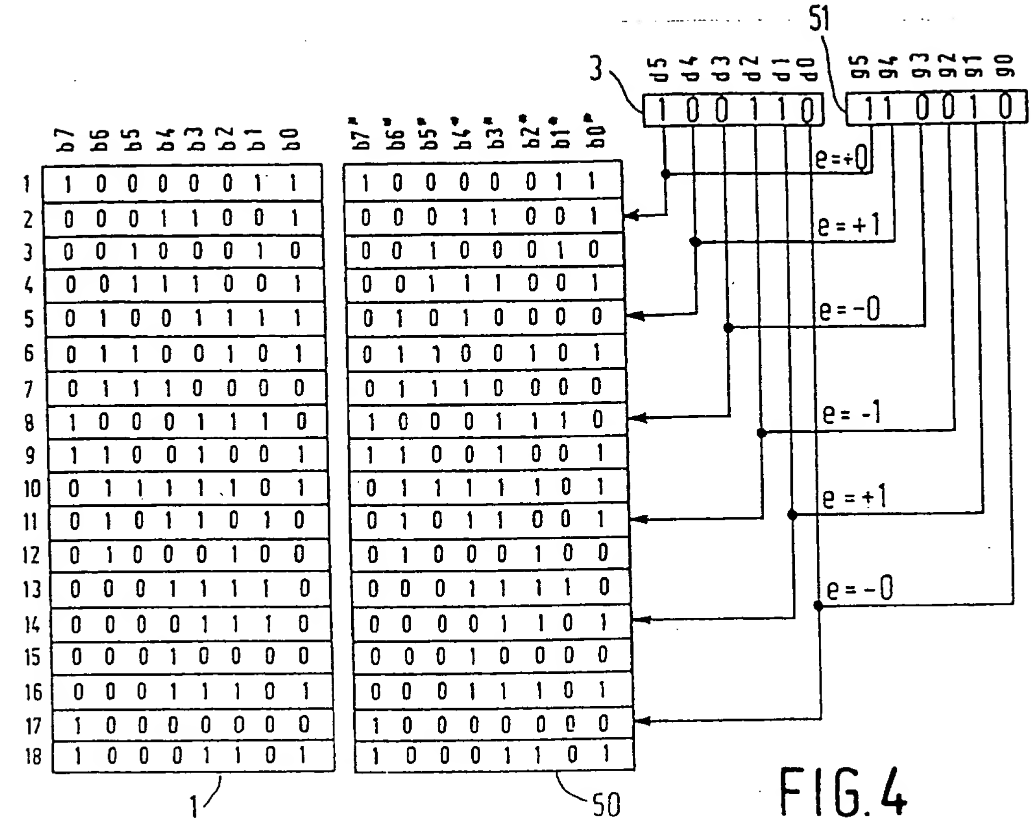
3
d5 d4 d3 d2 d1 d0
1 0 0 1 1 0
51
g5 g4 g3 g2 g1 g0
1 1 0 0 1 0
b7 b6 b5 b4 b3 b2 b1 b0
b7* b6* b5* b4* b3* b2* b1* b0*
1 1 0 0 0 0 0 1 1 | 1 0 0 0 0 0 1 1
2 0 0 0 1 1 0 0 1 | 0 0 0 1 1 0 0 1
3 0 0 1 0 0 0 1 0 | 0 0 1 0 0 0 1 0
4 0 0 1 1 1 0 0 1 | 0 0 1 1 1 0 0 1
5 0 1 0 0 1 1 1 1 | 0 1 0 1 0 0 0 0
6 0 1 1 0 0 1 0 1 | 0 1 1 0 0 1 0 1
7 0 1 1 1 0 0 0 0 | 0 1 1 1 0 0 0 0
8 1 0 0 0 1 1 1 0 | 1 0 0 0 1 1 1 0
9 1 1 0 0 1 0 0 1 | 1 1 0 0 1 0 0 1
10 0 1 1 1 1 1 0 1 | 0 1 1 1 1 1 0 1
11 0 1 0 1 1 0 1 0 | 0 1 0 1 1 0 0 1
12 0 1 0 0 0 1 0 0 | 0 1 0 0 0 1 0 0
13 0 0 0 1 1 1 1 0 | 0 0 0 1 1 1 1 0
14 0 0 0 0 1 1 1 0 | 0 0 0 0 1 1 0 1
15 0 0 0 1 0 0 0 0 | 0 0 0 1 0 0 0 0
16 0 0 0 1 1 1 0 1 | 0 0 0 1 1 1 0 1
17 1 0 0 0 0 0 0 0 | 1 0 0 0 0 0 0 0
18 1 0 0 0 1 1 0 1 | 1 0 0 0 1 1 0 1
e=+0
e=+1
e=-0
e=-1
e=+1
e=-0
1
50

FIG.4

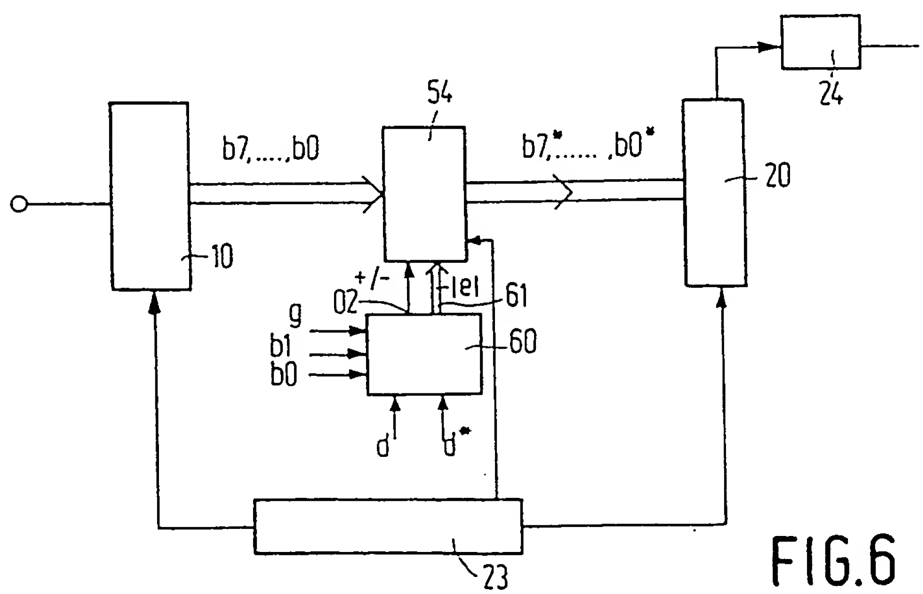
b7,.....,b0
54
b7*,......,b0*
24
20
10
+/-
02
|e|
61
g
b1
b0
60
d
d*
23

FIG.6